ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a memory cell, and first and second capacitive elements. The memory cell has a pair of inverters each including first and second driver nMOS transistors and first and second TFTs, and first and second access nMOS transistors. The first and second capacitive elements is connected to the drain of first and second access nMOS transistors, the drain of first and second driver nMOS transistors, and the drain of first and second TFTs. The gate width of first and second driver nMOS transistors is set at least 1.2 times longer than the gate width of first and second access nMOS transistors.